

# Operating Manual

## Lock-In Amplifier Module Series LIA-MV(D)-200



© 9/2018  
Rev. 6



## Table of Contents

<b>1</b>	<b>INTRODUCTION</b>	<b>4</b>
<b>2</b>	<b>MODELS OF THE LIA-MV(D)-200 SERIES</b>	<b>4</b>
<b>3</b>	<b>ABSOLUTE MAXIMUM RATINGS</b>	<b>5</b>
<b>4</b>	<b>SPECIFICATIONS</b>	<b>5</b>
<b>5</b>	<b>STANDARD CONFIGURATION OF THE LOCK-IN AMPLIFIER (FACTORY SETTINGS)</b>	<b>8</b>
5.1	Amplifiers without Optional SOM-1 Module	8
5.2	Amplifiers with Optional SOM-1 Module	8
<b>6</b>	<b>GETTING READY TO USE THE LIA-MV(D)-200</b>	<b>9</b>
<b>7</b>	<b>MANUAL OPERATION</b>	<b>9</b>
7.1	LED Indications	10
7.2	Gain and Dynamics	10
7.3	Adjusting the Phase	14
7.3.1	Phase Shifter Resolution of 8 Bit	14
7.3.2	Phase Shifter Resolution of 7 Bit	15
7.4	2f-Mode	15
7.5	Time Constant and Filter Characteristics	16
7.6	DIP Switches S1-S4	17
<b>8</b>	<b>OPERATION WITH CONTROL INTERFACE</b>	<b>18</b>
8.1	Assignment of the SUB-D 25 Pin Socket	18
8.2	Overview of all Digitally Controllable Functions	19
<b>9</b>	<b>MIXED OPERATION</b>	<b>22</b>

---

<b>10</b>	<b>ADVANCED CONFIGURATION OF THE LOCK-IN AMPLIFIER</b>	<b>22</b>
10.1	Opening and Closing the Device	22
10.2	Optional Sine-Oscillator-Module SOM-1	23
10.3	Modification of the Input Signal Filters	24
10.4	Setting the Working Frequency Range (H-Models Only)	24
10.5	Changing the Assignment of the BNC Sockets	26
10.5.1	Options for the Assignment of the BNC Socket “REFERENCE INPUT”	27
10.5.2	Options for the Assignment of the BNC Socket “SIGNAL INPUT”	28
10.5.3	Options for the Assignment of the “OUTPUT” BNC Sockets	29
<b>11</b>	<b>DIMENSIONS</b>	<b>30</b>
<b>12</b>	<b>BLOCK DIAGRAM</b>	<b>31</b>

## 1 Introduction

Lock-in amplifiers are used to measure weak signals which may be hidden in background noise of much higher amplitude than the actual signal that needs to be measured.

A lock-in amplifier is essentially a frequency and phase sensitive AC-voltmeter which allows detecting a weak signal at a specific frequency and phase which is provided by a reference source.

FEMTO's LIA-MV(D)-200 Series Lock-In Amplifier Modules cover a wide frequency range up to 120 kHz. The input can be configured as voltage or current input and the sensitivity can be varied over a wide range. For adjusting the phase a digital phase shifter is included with a resolution of 1.4°. Further control elements for setting the time-constant, dynamic reserve, 1f/2f mode and the reference signal characteristic are provided as well. All functions can be controlled locally by manual switches or by the digital remote interface with TTL/CMOS control signals. Therefore the device is ideally suited for use as a stand-alone unit or as part of a complex measuring system.

The miniature module LIA-MV-150 with even smaller dimensions and the 19"-board version LIA-BV(D)-150 complete FEMTO's spectrum of lock-in amplifiers for use in scientific or industrial applications.

## 2 Models of the LIA-MV(D)-200 Series

The LIA-MV(D)-200 Series Lock-In Amplifier Modules are complete single phase or dual phase lock-in amplifiers in a robust aluminum housing.

The following models are available:

LIA-MV-200-L	-	single phase, working frequency	5 Hz ... 10 kHz
LIA-MV-200-H	-	single phase, working frequency	50 Hz ... 120 kHz
LIA-MVD-200-L	-	dual phase, working frequency	5 Hz ... 10 kHz
LIA-MVD-200-H	-	dual phase, working frequency	50 Hz ... 120 kHz

While single phase units only offer the X signal which is in phase with the reference signal the dual phase models also offer Y (90° phase shifted with respect to the reference signal) and R signals (magnitude, vector sum of X and Y). Please note when using a LIA-MVD-200 dual phase lock-in amplifier that due to the square wave mixer used inside the lock in a true phase independent measurement is only possible for a sinusoidal input signal. If your input signal has a different form the R output may still show a moderate phase dependence.

The basic specifications of the four models are similar. Differences or extended specifications are outlined in this manual.

The optionally available Sine-Oscillator Module SOM-1 provides an internal reference signal.

### 3 Absolute Maximum Ratings

Supply Voltage:	$\pm 22$ V
Signal Input Voltage AC:	50 V <sub>PP</sub>
Reference Input Voltage:	$\pm 15$ V
Logic-Inputs:	-5 ... +15 V

Exceeding the absolute maximum ratings may result in damage to the lock-in amplifier.

### 4 Specifications

#### Voltage Signal Input

Configuration:	instrumentation amplifier, true-differential
Voltage Range (Full Scale):	3 $\mu$ V <sub>rms</sub> to 1 V <sub>rms</sub> (switchable in 1-3-10 steps)
Coupling:	AC
Gain Drift:	< 100 ppm/ K
Input Impedance:	1 M $\Omega$    4 pF
Voltage Noise:	12 nV/ $\sqrt$ Hz
Common Mode Rejection Ratio (CMRR):	110 dB @ 1 kHz, 100 dB @ 10 kHz

#### Current Signal Input

Configuration:	transimpedance amplifier, -100 kV/A, (inverting)
Current Range (Full Scale):	30 pA <sub>rms</sub> to 10 $\mu$ A <sub>rms</sub> (switchable in 1-3-10 steps)
Coupling:	DC
Current Noise:	0.4 pA/ $\sqrt$ Hz
Source Capacitance:	10 pF – 500 pF

#### Signal Input Filter

Adjustment:	cut-off frequencies (-3 dB) via internal jumpers
Upper-Cut-Off-Frequencies:	100 Hz / 1 kHz / 10 kHz / 100 kHz / 1 MHz
Lower-Cut-Off-Frequencies:	Model -L: 0.2 Hz / 1 Hz / 10 Hz / 100 Hz / 1 kHz Model -H: 2 Hz / 10 Hz / 100 Hz / 1 kHz / 10 kHz
Characteristic:	6 dB / Octave
Frequency Accuracy:	$\pm 20$ %

#### Reference Input

Input Voltage Range:	bipolar: $\pm 100$ mV to $\pm 5$ V (comparator threshold: 0 V) TTL: -5 V to +10 V (comparator threshold: +2 V)
Input Impedance:	1 M $\Omega$    10 pF
Acquisition Time	
Slow Setting:	4 s max.
Fast Setting:	2 s max.

### Phase

Adjustment Range:	0 - 360°, digitally controlled
Resolution:	1.4° (8 bit) or 2.8° (7 bit) drift: < 100 ppm / K
Accuracy:	> 0.3°
Orthogonality:	< 0.1°

### Dynamic Reserve

Demodulator:	15 dB @ “ultra-stable” setting 35 dB @ “low drift” setting 55 dB @ “high dynamic” setting
--------------	---

### Output

Output Channels:	X – in phase Y – quadrature (dual phase models only) R – magnitude (dual phase models only)
Output Voltage:	±10 V @ > 2 kΩ load
Output Current:	±5 mA max.
Impedance:	50 Ω (terminate with load > 10 kΩ for best results)
DC-Drift:	5 ppm / K @ “ultra-stable” setting 50 ppm / K @ “low drift” setting 500 ppm / K @ “high dynamic” setting
Basic Accuracy:	2 % (X and Y output) for sinusoidal input signal
Vector-Sum Accuracy:	4 % (dual phase models only) for sinusoidal input signal
Output Offset Range:	±100 % full scale with ±10 V control voltage

### Signal Monitor Output

Monitor Gain:	1 – 3333, depends on AC signal amplification
Monitor Output Voltage Range:	±8 V max.
Monitor Output Impedance:	100 Ω
Monitor Output Current:	±10 mA max.

### Time Constants

Range:	model –L: 3 ms to 10 s (switchable in 1-3-10 steps) model –H: 300 μs to 1 s (switchable in 1-3-10 steps)
Filter-Characteristic:	6 dB or 12 dB/octave switchable

### Digital Control

Control Voltage	high: +1.8 V ... +12 V low: –0.8 V ... +0.8 V
Control Current	0 mA @ 0V; 1.5 mA @ +5 V; 4.5 mA @ +12 V typ.
Output Voltage	active: +4.5 V typ. non active: 0 V typ.

Output Current: 10 mA max.  
LED Indications: overload, unlocked and power

**Power Supply**

Supply Voltage:  $\pm 15$  VDC min.  
 $\pm 18$  VDC max.  
Supply Current: +120 mA; -60 mA typ. (depends on operating conditions, recommended power supply capability minimum  $\pm 150$  mA)

**Temperature Range**

Operating: 0 °C ... +50 °C  
Storage: -40 °C ... +100 °C

**Dimensions and Weight**

Dimensions: 105 mm x 223 mm x 64 mm  
(without BNC sockets)  
Weight: approx. 1000 g (2.2 lbs)

## 5 Standard Configuration of the Lock-In Amplifier (Factory Settings)

### 5.1 Amplifiers without Optional SOM-1 Module

Standard factory settings are as follows:

- The BNC socket “SIGNAL INPUT” is configured as single ended AC coupled voltage input
- The output signal is available as in-phase signal at the BNC terminal “OUTPUT X”. In addition the dual phase models LIA-MVD-200 provide quadrature and vector-sum outputs at “OUTPUT Y” and “OUTPUT R”, respectively.
- The lower cut-off input signal filter is set to 0.2 Hz for L-models and to 2.0 Hz for H-models. The upper cut-off frequency is set to > 1 MHz for both models.
- The working frequency range for L-models is 5 Hz...10 kHz, 1f-mode and 2f-mode are possible. The phase shifter resolution is 8 bit at 1f-mode and 7 bit at 2f-mode.  
The working frequency range for H-models is set to 50 Hz...120 kHz, only 1f-mode is supported (DIP switch S2 is without function in this setting). The phase shifter resolution is 7 bit.
- The signal monitor output is not externally available.
- The external reference voltage must be fed to the BNC socket “Reference INPUT”

To change the standard configuration see chapter 9.

### 5.2 Amplifiers with Optional SOM-1 Module

The lock-in amplifiers can be equipped with the optional SOM-1 reference signal module. The standard configuration is similar to the one described in chapter 5.1 except for the BNC socket “REFERENCE INPUT” which now functions as output socket.

The internal SOM-1 module generates a sine wave reference signal. It is directly connected to the internal lock-in reference input. Factory set to 1 kHz and 1 V<sub>rms</sub> this reference signal is also available at the BNC terminal “REFERENCE INPUT” for external use.



## 6 Getting Ready to Use the LIA-MV(D)-200

The LIA-MV(D)-200 requires a DC supply voltage of  $\pm 15\text{ V}$  connected to the 3-Pin LEMO socket on the backside of the amplifier.

We recommend using the PS-15 FEMTO power supply as it is designed for optimum performance of the lock-in amplifier.

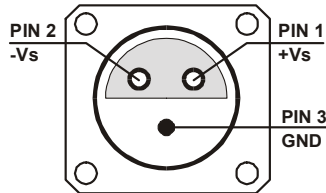


Figure 1: 3-Pin-LEMO Socket

The positive and negative supply voltages should be switched on simultaneously.

In order to avoid noise pickup you should use a coaxial cable to connect the signal source or the preamplifier to the lock-in signal input. The factory setting for the input is an AC coupled voltage input configuration. For changing this setting please see chapter 9.

An external reference signal needs to be connected to the BNC socket “REFERENCE INPUT”. Please use coaxial cables for the reference signal as well and make sure that the signal is in the correct voltage and frequency range. If you ordered a lock-in amplifier with optional SOM-1 reference oscillator the reference signal is generated internally and can be picked up at the BNC socket labeled “REFERENCE INPUT” for external use in your set-up.

Finally, the signal outputs should be connected using coaxial cables to a voltmeter, analog/digital converter, oscilloscope or similar.

## 7 Manual Operation

The parameters of the lock-in amplifier are controlled by four hexadecimal switches (0 – F) and four DIP switches on the front panel.

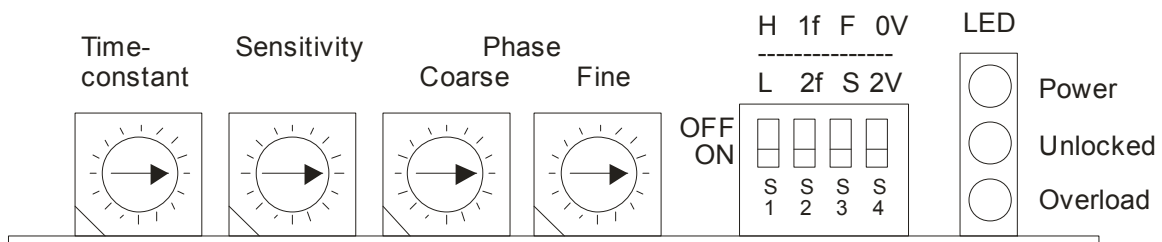


Figure 2: View of the front panel switches

### 7.1 LED Indications

The LEDs on the front panel provide the status information:

Power (green)	power supply on
Overload (red)	noise level too high, dynamic reserve not sufficient, incorrect gain range
Unlocked (red)	PLL not locked, reference signal not connected or out of range

### 7.2 Gain and Dynamics

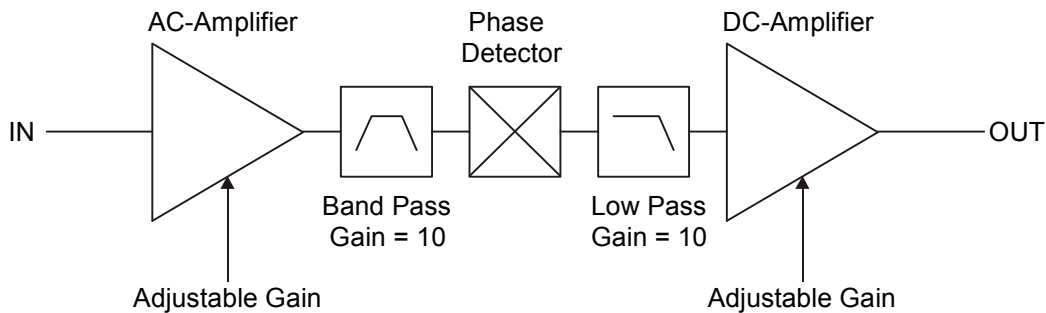


Figure 3: Block diagram

The block diagram shows the path along the involved stages:

- AC-amplifier – amplifies the input signal for further processing along the lock-in signal path.
- Input band pass filter with adjustable upper and lower frequency limits – useful for eliminating strong noise or perturbation components.
- Phase detector – this is the core of the lock-in amplifier which multiplies the input signal (including the noise) with the reference signal. This process is also known as mixing and translates the actual signal at the reference frequency down to DC level.
- Low pass filter with adjustable time constant – responsible for eliminating all non-DC components and for smoothing the output.
- DC-amplifier – amplifies the smoothed signal to the desired output level.

The gain of the AC-amplifier at the signal input and the gain of the DC-amplifier at the output can be adjusted via the hexadecimal switch “Sensitivity” (settings  $0_{hex}$  to  $F_{hex}$ ) and via the DIP switch S1 “Dynamic Reserve” on the front panel.

A very important parameter is the required dynamic reserve which is the ratio of the largest tolerable noise level to the signal for full scale output. For example, if the lock-in is set to a sensitivity of  $10 \mu V$  for a full scale output a dynamic reserve of 40 dB means that the noise level can go up to 1 mV (= 40 dB equals a factor of 100) without overloading the amplifier. In this setting a  $10 \mu V_{rms}$  input signal covered in up to 1 mV noise will result in the full scale output of the lock-in amplifier (10 V DC at the output). Even smaller input signals can be measured in this setting. In our example an input signal of  $1 \mu V_{rms}$  will result in an output signal of 1 V DC even if the noise level is still 1 mV at the input.

A certain amount of overall gain can be achieved either by high AC-amplification and low DC-amplification or by low AC-amplification and high DC-amplification. However, the consequences with respect to DC-stability are contrary and require a careful selection of the settings. For LIA-MV(D)-200 lock-in amplifiers offer 3 different modes of best possible compromise between dynamic reserve and applications:

- High Dynamic Reserve – for small signals with high dynamic reserve in this setting is at least 55 dB; the DC drift is 500 ppm/K.
- Low Drift – for medium signals with medium noise level; the dynamic reserve is 35 dB; the DC drift is 50 ppm/K; this mode is achieved by combinations of switch settings as described in table 1.
- Ultra-Stable – for a very stable output signal; the DC drift is 5 ppm/K; the dynamic reserve is 15 dB.

高交流放大率和低直流放大率或低交流放大率和高直流放大率可以实现一定量的总增益。但是，直流稳定性和动态储备的后果是相反的，需要仔细选择设置。因此，LIA-MV(D)-200系列锁定放大器提供3种不同的工作模式，以在各种应用中动态保留和输出稳定性之间实现最大可能的折衷：  
 • 高动态储备 - 适用于高噪声水平的小信号；在此设置下的动态保留至少为55 dB；直流漂移为500 ppm / K。  
 • 低漂移 - 适用于中等噪声水平的中等信号；动态储备为35 dB；直流漂移为50 ppm / K；如下表1所述，可以通过两种不同的开关设置组合来实现此模式。  
 • 超稳定 - 产生非常稳定的输出信号；DC漂移极佳，仅为5 ppm / K；动态储备为15 dB。

The following parameters determine the distribution of the overall gain to the various stages. Table 1 lists these parameters for the 3 different modes of operation:

- Input level of the signal of interest  
The level of the signal to be measured is usually determined by the circumstances of the measurement set-up. The “Input Signal” show the maximum input level for linear operation without overload. This maximum input level will be 10 V.
- The required output level  
The output level is usually determined by the instrument for signal analysis (e.g. DC voltmeter, A/D converter). Typical values of the output level are in the range of 1...10 V.
- Stability of the output  
The stability of the lock-in output is mainly determined by the drift of the DC-amplifier. To optimize the stability of the amplification should be kept as low as possible. The temperature drift is thus minimized.
- Maximum dynamic reserve  
As outlined above the dynamic reserve is a measure of the lock-in’s ability to recover signals that are buried in noise. For measurements with high noise levels or other spectral components which cannot be rejected by the adjustable band pass filter ahead of the phase detector the dynamic reserve should be increased to guarantee that the actual signal can be extracted from the noise components.

以下参数确定总增益在各个阶段的分布。表1列出了3种不同操作模式下的这些参数：  
 • 感兴趣信号的输入电平：待测信号的电平通常取决于测量设置的情况。“输入信号”列中的数字显示了在没有过载的情况下线性锁定的最大输入电平。此最大输入电平将导致10 V的满量程输出。  
 • 所需的输出电平：输出电平通常由锁定分析信号后的仪器（例如，直流电压表，A / D转换器或示波器）确定。输出电平的典型值在1...10 V范围内。  
 • 输出的稳定性：锁定输出的稳定性主要取决于直流放大器的直流温度漂移。为了优化输出电平的稳定性，除非受到其他参数的限制，否则直流放大应保持尽可能低的水平。因此温度漂移最小。  
 • 最大动态储备：如上文所述，动态储备是锁定功能恢复埋在噪声中的信号的能力的度量。对于具有高噪声水平或其他频谱分量的测量，这些噪声不能被相位检测器之前的可调带通滤波器拒绝，则应增加动态储备，以确保可以从噪声分量中提取出实际信号。

We recommend starting with the “Ultra-Stable” mode if high noise is not expected. In this setting the value of the noise signals can be still 6 times (15 dB) higher than the selected sensitivity setting. An adjustment of the phase shifter should be performed to ensure that the output signal reached the maximum possible value.

If despite of a low output signal level the “Overload-LED” is lit the phase detector might be overloaded due to high noise components. In this case switch to the “Low

Drift” or “High Dynamic Reserve” modes to increase the dynamic reserve and to avoid an overload of the phase detector by noise signals. This will result in lower output stability though as the temperature drift increases.

If the “Overload-LED” is on even in the “High Dynamic” mode with the output not yet reaching 10 V an extremely high interfering or noise signal has been picked up and the lock-in amplifier is not able to work properly. In this case check carefully all connections between the lock-in amplifier and the signal source, especially screening and grounding. Additionally a modification or adjustment of the switchable low and high pass filter may cure the problem (see chapter 9 for details).

For the single phase models LIA-MV-200 a phase adjustment is necessary to achieve best performance and to select the optimum sensitivity setting (see the following chapter 7.3). For the dual phase models LIA-MVD-200 a phase adjustment is recommended if the input signal is not of sinusoidal shape as otherwise the square wave mixer used inside the lock-in will not produce optimum results (see also chapter 2). 如果不希望出现高噪音，建议从“超稳定”模式开始。

在此设置中，噪声信号的值仍可以比所选灵敏度设置高6倍（15 dB）。应该对移相器进行调整，以确保输出信号达到最大可能值。

如果尽管输出信号电平较低，但“Overload-LED”点亮，则由于高噪声成分，相位检测器可能过载。在这种情况下，请切换到“Low漂移”或“高动态储备”模式，以增加动态储备并避免噪声信号使鉴相器过载。尽管随着温度漂移的增加，这将导致较低的输出稳定性。

如果即使在“高动态”模式下，“过载LED”仍亮着，而输出仍未达到10 V，则说明拾取了极高的干扰或噪声信号，并且锁相放大器无法正常工作。在这种情况下，请仔细检查锁定放大器和信号源之间的所有连接，尤其是屏蔽和接地。另外，对可切换的低通和高通滤波器进行修改或调整可以解决该问题（有关详细信息，请参阅第9章）。

对于单相型号LIA-MV-200，必须进行相位调整才能获得最佳性能并选择最佳灵敏度设置（请参阅以下第7.3章）。对于双相型号LIA-MVD-200，如果输入信号不是正弦波形状，则建议进行相位调整，否则锁相器内使用的方波混频器将不会产生最佳效果（另请参见第2章）。

The following table 1 lists the main parameters of the lock-in amplifier for the 3 different modes of operation and in dependence of the selected sensitivity setting.

Mode	Characteristics	Input Signal (rms) for Full Scale Output		Total Gain	Gain		Switch Setting	
		Voltage	Current		AC-Gain	DC-Gain	Hex Switch	DIP Switch S1
High Dynamic Reserve	Small signal	3 $\mu$ V	30 pA	$3 \times 10^6$	300.0	100	F <sub>HEX</sub>	H
	high noise level	10 $\mu$ V	100 pA	$1 \times 10^6$	100.0	100	E <sub>HEX</sub>	H
	dynamic reserve 55 dB	30 $\mu$ V	300 pA	$3 \times 10^5$	30.0	100	D <sub>HEX</sub>	H
	DC-drift 500 ppm/K	100 $\mu$ V	1 nA	$1 \times 10^5$	10.0	100	C <sub>HEX</sub>	H
		300 $\mu$ V	3 nA	$3 \times 10^4$	3.0	100	B <sub>HEX</sub>	H
		1 mV	10 nA	$1 \times 10^4$	1.0	100	A <sub>HEX</sub>	H
		3 mV	30 nA	$3 \times 10^3$	0.3	100	9 <sub>HEX</sub>	H
		10 mV	100 nA	$1 \times 10^3$	0.1	100	8 <sub>HEX</sub>	H
Low Drift	medium signal	30 $\mu$ V	300 pA	$3 \times 10^5$	300.0	10	7 <sub>HEX</sub>	H
	medium noise level	100 $\mu$ V	1 nA	$1 \times 10^5$	100.0	10	6 <sub>HEX</sub>	H
	dynamic reserve 35 dB	300 $\mu$ V	3 nA	$3 \times 10^4$	30.0	10	5 <sub>HEX</sub>	H
	DC-drift 50 ppm/K	1 mV	10 nA	$1 \times 10^4$	10.0	10	4 <sub>HEX</sub>	H
		3 mV	30 nA	$3 \times 10^3$	3.0	10	3 <sub>HEX</sub>	H
		10 mV	100 nA	$1 \times 10^3$	1.0	10	2 <sub>HEX</sub>	H
		30 mV	300 nA	$3 \times 10^2$	0.3	10	1 <sub>HEX</sub>	H
		100 mV	1 $\mu$ A	$1 \times 10^2$	0.1	10	0 <sub>HEX</sub>	H
		30 $\mu$ V	300 pA	$3 \times 10^5$	300.0	10	F <sub>HEX</sub>	L
		100 $\mu$ V	1 nA	$1 \times 10^5$	100.0	10	E <sub>HEX</sub>	L
		300 $\mu$ V	3 nA	$3 \times 10^4$	30.0	10	D <sub>HEX</sub>	L
		1 mV	10 nA	$1 \times 10^4$	10.0	10	C <sub>HEX</sub>	L
		3 mV	30 nA	$3 \times 10^3$	3.0	10	B <sub>HEX</sub>	L
		10 mV	100 nA	$1 \times 10^3$	1.0	10	A <sub>HEX</sub>	L
		30 mV	300 nA	$3 \times 10^2$	0.3	10	9 <sub>HEX</sub>	L
		100 mV	1 $\mu$ A	$1 \times 10^2$	0.1	10	8 <sub>HEX</sub>	L
Ultra-Stable	high signal	300 $\mu$ V	3 nA	$3 \times 10^4$	300.0	1	7 <sub>HEX</sub>	L
	small noise level	1 mV	10 nA	$1 \times 10^4$	100.0	1	6 <sub>HEX</sub>	L
	dynamic reserve 15 dB	3 mV	30 nA	$3 \times 10^3$	30.0	1	5 <sub>HEX</sub>	L
	DC-drift 5 ppm/K	10 mV	100 nA	$1 \times 10^3$	10.0	1	4 <sub>HEX</sub>	L
		30 mV	300 nA	$3 \times 10^2$	3.0	1	3 <sub>HEX</sub>	L
		100 mV	1 $\mu$ A	$1 \times 10^2$	1.0	1	2 <sub>HEX</sub>	L
		300 mV	3 $\mu$ A	$3 \times 10^1$	0.3	1	1 <sub>HEX</sub>	L
		1 V	10 $\mu$ A	$1 \times 10^1$	0.1	1	0 <sub>HEX</sub>	L

Table 1: Gain and Dynamics LIA-MV(D)-200

### 7.3 Adjusting the Phase

The correct phase adjustment between the input signal and the reference signal is very important in order to obtain maximum output signals.

The phase can be adjusted with the hexadecimal-code switches. For the LIA-MV(D)-200 models the "Y-OUTPUT" will reach a value of 0 when X and Y are phase shifted by 90°. If the input signal has a sine wave shape, the "ROUTPUT" of dual phase models automatically delivers the maximum output signal without the need for phase adjustment. If the signal is not a sine wave, the "ROUTPUT" will show a phase dependence which might be reduced by filtering. Please contact FEMTO for details.

为了获得最大的输出信号，输入信号和参考信号之间的正确相位调整非常重要。可以使用十六进制代码开关“Coarse”和“Fine”调整相位，以在“X-OUTPUT”处获得最大输出信号。对于LIA-MVD-200双相模型，“Y输出”将达到接近零的值，因为X和Y相移了90°。如果输入信号具有正弦曲线形状，则双相模型的“ROUTPUT”会自动提供最大的输出信号，而无需进行相位调整。如果信号不是正弦波，则“ROUTPUT”将显示相位相关性，可通过进一步的信号滤波来降低相位相关性。请联系FEMTO了解详细信息。该相位可通过两个十六进制代码开关进行总共256步的调整。开关的位置被编码为从0到255的8位字，分别对应于00Hex ... FFHex。根据锁相放大器的配置和所选的工作模式，移相器可提供0位或7位分辨率（左页标准配置）。

The phase is adjustable with the two hex-code switches in a total of 256 steps. The positions of the switches are encoded as an 8-bit word from 0 to 255, corresponding to 00<sub>Hex</sub>...FF<sub>Hex</sub>, respectively.

Depending on the configuration of the lock-in amplifier and the chosen operating mode the phase shifter provides either 8 or 7 bit resolution (for standard configuration see chapter 5).

#### 7.3.1 Phase Shifter Resolution of 8 Bit

The code-switches "Coarse" and "Fine" enable 22.5° and 1.4° resolution respectively.

The 8 bit resolution is available for the following models and modes:

- L-models with standard configuration in 1f-mode.
- H-models with modified configuration for a maximum working frequency of 60 kHz in 1f-mode (for changing the standard configuration please see chapter 9).

代码开关“粗略”和“精细”分别启用22.5°和1.4°分辨率。8位分辨率可用于以下型号和操作模式：  
 •标准配置为1f模式的L型。  
 •修改后配置的H型在1f模式下的最大工作频率为60 kHz（有关更改标准配置，请参见第9章）。  
 如果将移相器设置为8位分辨率，则可以如下计算相位：

If the phase shifter is set to 8 bit resolution the phase can be calculated as follows:

$$\text{Phase} = 360 \cdot \frac{\text{CODE}_{\text{DEC}}}{256}$$

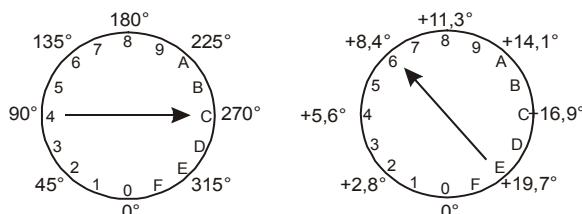


Figure 4: The shown position is C6<sub>HEX</sub> equivalent to 198<sub>DEC</sub>. Using above formula the phase is calculated as 278.4°.

In a less mathematical way the code-switch "Coarse" represents directly the geometrical angle of the phase whereas the code switch "Fine" is used for the fine calibration.

### 7.3.2 Phase Shifter Resolution of 7 Bit

In this mode the code-switches “Coarse” and “Fine” enable 45° and 2.8 ° resolution, respectively.

The 7 bit resolution is available for the following models and operating modes:

- L-models with standard configuration in 2f-mode.
- H-models with standard configuration.
- H-models with modified configuration for a maximum working frequency of 60 kHz in 2f-mode (for changing the standard configuration please see chapter 9).

If the phase shifter is set to 7 bit resolution the phase can be calculated as follows:

$$\text{Phase} = 360 \cdot \frac{\text{CODE}_{\text{DEC}}}{128}$$

In a less mathematical way the geometrical angle of the code-switch “Coarse” represents half of the adjusted phase angle (45° geometrical angle = 90° phase angle) whereas the code-switch “Fine” is used for the fine calibration.

Table 2 shows a few examples of different phase shifter settings and corresponding phase values.

Code		Phase	
HEX	DEC	8 bit	7 bit
00 <sub>HEX</sub>	0 <sub>DEC</sub>	0°	0°
20 <sub>HEX</sub>	32 <sub>DEC</sub>	45°	90°
40 <sub>HEX</sub>	64 <sub>DEC</sub>	90°	180°
60 <sub>HEX</sub>	96 <sub>DEC</sub>	135°	270°

Code		Phase	
HEX	DEC	8 bit	7 bit
80 <sub>HEX</sub>	128 <sub>DEC</sub>	180.00°	360.0°
08 <sub>HEX</sub>	8 <sub>DEC</sub>	11.25°	22.5°
0C <sub>HEX</sub>	12 <sub>DEC</sub>	16.90°	33.8°
E0 <sub>HEX</sub>	224 <sub>DEC</sub>	315.00°	630.0°

Table 2: Examples of phase settings (8 bit and 7 bit resolution)

### 7.4 2f-Mode

The LIA-MV(D)-200 Series Lock-In Amplifiers allow for the use of the 2f-mode.

In 2f-mode the lock-in amplifier detects the signal components at the second harmonic of the reference frequency. This mode is useful for measuring the harmonic content of a signal e.g. in resonance absorption measurements. When the 2f-mode is selected with DIP switch S2 the reference frequency will be internally doubled and the resolution of the phase shifter will be reduced to 7 bit (see chapter 7.3.2).

**Attention:** In standard configuration 2f-mode is only available for L-models. To use this mode with H-models a modified configuration is necessary (see chapter 9 for details).

### 7.5 Time Constant and Filter Characteristics

The choice of the time constant is always a compromise between noise suppression and measurement time.

Increasing the time constant will result in a more accurate and less noisy output signal of the lock-in amplifier. At the same time the measurement period will increase as well as it takes more time to reach a stable output signal. The amount of fluctuations on the output signal is inverse proportional to the chosen time constant.

The measurement period is proportional to the time constant. As a rule of thumb it is advised to wait ca. five times the set time constant before reading the lock-in output in order to achieve an accurate and stable output signal. The accuracy is dependent on the measurement period and can be described by the following formula:

$$\text{Error in \%: } \delta = 100 \times \exp(-t/\tau) \quad \begin{array}{l} t = \text{measurement time,} \\ \tau = \text{lock-in time-constant} \end{array}$$

Example: If you chose a time constant of 1 s with the hexadecimal switch on the front panel you should wait ca. 5 s before reading the signal at the output of the lock-in. During this time the output signal will approach its final end-value. After 1 s the lock-in output will have reached 63 % of the end-value and the remaining error is 37%. After 2 s the error is 14 % and after 3 s only 5 %. After 5 s the lock-in output will have an error of less than 1 % with respect to the final end-value you would achieve after an infinite measurement period.

For setting the time-constant a low pass filter with either a 12 dB/octave or a 6 dB/octave characteristic can be chosen. Usually the 12 dB/octave characteristic should be used because of the much better noise performance. Only in closed-loop systems where stability is very important and may be negatively influenced by the second order filter the 6 dB/octave characteristic is more useful.

The time constant of the output low pass filter is selected by the hexadecimal switch “Time Constant”.

Time constant Model “-L”	Time constant Model “-H”	Hexadecimal switch	
		6dB/Octave	12dB/Octave
3 ms	300 μs	0 <sub>HEX</sub>	8 <sub>HEX</sub>
10 ms	1 ms	1 <sub>HEX</sub>	9 <sub>HEX</sub>
30 ms	3 ms	2 <sub>HEX</sub>	A <sub>HEX</sub>
100 ms	10 ms	3 <sub>HEX</sub>	B <sub>HEX</sub>
300 ms	30 ms	4 <sub>HEX</sub>	C <sub>HEX</sub>
1 s	100 ms	5 <sub>HEX</sub>	D <sub>HEX</sub>
3 s	300 ms	6 <sub>HEX</sub>	E <sub>HEX</sub>
10 s	1 s	7 <sub>HEX</sub>	F <sub>HEX</sub>

Table 3: Time constants



## 7.6 DIP Switches S1-S4

The 4 DIP switches shown in figure 2 control the following operating parameters:

- DIP switch S1** Choice of high or low dynamic reserve. In combination with the “Sensitivity” hexadecimal switch the 3 modes of operation for the AC- and DC-amplifiers can be selected (see chapter 7.2)
- DIP switch S2** Enables either detection of the fundamental signal when switched to “off” (1f-mode) or detection of the second harmonic signal when switched to “on” (2f-mode).  
When using H-models in the standard configuration S2 is inoperative. To use 2f-mode with a H-model the internal jumper settings need to be changed (see chapter 9.4). Please note that the input fundamental signal as well as the maximum reference frequency is limited to 60 kHz (see chapter 7.3.2, 7.4 and 9.4)
- DIP switch S3** Determines the time the internal PLL (Phase-Locked-Loop) circuit requires to lock to the external reference signal. The two settings are:
- SLOW: („ON“) This is the most common setting which should be preferred if the measuring frequency is at a fix value. The phase is extraordinary stable in this setting.
- FAST: („OFF“) In frequency-sweeping measurements with an external oscillator sweeping relatively fast over a wide range (e.g. 100 Hz ... 10 kHz) best results are achieved with this setting.
- If the unlocked LED is “ON” the PLL is not locked. In this case make sure that the frequency and amplitude of your reference signal are within the specified ranges. For reference frequencies below 40 Hz we recommend the “slow” setting.
- DIP Switch S4:** Selects the threshold level for the reference comparator. For e.g. a sinusoidal reference signal centered around zero with a voltage of  $\pm 100$  mV...  $\pm 5$  V or analog reference signals without DC-shift the level should be set to “0 V”.  
If the reference signal is a digital signal (TTL, CMOS) the switch should be set to “2 V”.

Dip switch	Switch setting	
	OFF	ON
S1	Low Drift and High Dynamic Mode	Ultra-Stable and Low Drift Mode
S2	1f-Mode	2f-Mode
S3	PLL Fast Locking	PLL Slow Locking
S4	Threshold of Reference Input =0 V	Threshold of Reference Input =2 V

Table 4: DIP Switches

## 8 Operation with Control Interface

The LIA-MV(D)-200 Series Lock-In Amplifiers provide TTL/CMOS-compatible digital inputs which are isolated from the analog circuits by opto-couplers. The digital input levels must remain static during a measurement. The best choice for providing the TTL-bits and programming the lock-in amplifier is a standard PC I/O interface card with digital outputs. A high-level at the TTL-input presents a logical 1.

The digital inputs of the lock-in consist of 3 groups. The first group controls the phase shift. These 8 bits correspond, as described in chapter 7.3, to a binary number of 0 to 255. A second group of four bits controls the time constants and a third group of four bits manages the full scale sensitivity of the lock-in amplifier. Finally, there is one further digital input which can be used to disable the local hexadecimal switches on the front panel (see chapter 8.3).

The DIP switches cannot be remote controlled.

### 8.1 Assignment of the SUB-D 25 Pin Socket

Pin 1	+12 V (Stabilized Power Supply Output)
Pin 2:	-12 V (Stabilized Power Supply Output)
Pin 3:	AGND (Analog Ground)
Pin 4:	+5 V (Stabilized Power Supply Output)
Pin 5:	X-Output
Pin 6:	Overload Status Output
Pin 7:	Unlocked Status Output
Pin 8:	Disable Local Switch Control Input
Pin 9:	DGND (Ground for Digital Control Pins 8 - 25)
Pin 10:	Dynamic Mode (DYN0)
Pin 11:	Sensitivity (SEN0)
Pin 12:	Sensitivity (SEN1)
Pin 13:	Sensitivity (SEN2)
Pin 14:	Time Constant Slope (TCSL)
Pin 15:	Time Constant (TC0)
Pin 16:	Time Constant (TC1)
Pin 17:	Time Constant (TC2)
Pin 18:	Phase Shift (PH0)
Pin 19:	Phase Shift (PH1)
Pin 20:	Phase Shift (PH2)
Pin 21:	Phase Shift (PH3)
Pin 22:	Phase Shift (PH4)
Pin 23:	Phase Shift (PH5)
Pin 24:	Phase Shift (PH6)
Pin 25:	Phase Shift (PH7)

## 8.2 Overview of all Digitally Controllable Functions

Time Constants				6/12 dB Octave	T.C. MSB	T.C.	T.C. LSB
HEX	Time constant Model “-L”	Time constant Model “-H”	Filter characteristic	Pin 14	Pin 17	Pin 16	Pin 15
0	3 ms	300 $\mu$ s	6 dB	Low	Low	Low	Low
1	10 ms	1 ms	6 dB	Low	Low	Low	High
2	30 ms	3 ms	6 dB	Low	Low	High	Low
3	100 ms	10 ms	6 dB	Low	Low	High	High
4	300 ms	30 ms	6 dB	Low	High	Low	Low
5	1 s	100 ms	6 dB	Low	High	Low	High
6	3 s	300 ms	6 dB	Low	High	High	Low
7	10 s	1 s	6 dB	Low	High	High	High
8	3 ms	300 $\mu$ s	12 dB	High	Low	Low	Low
9	10 ms	1 ms	12 dB	High	Low	Low	High
A	30 ms	3 ms	12 dB	High	Low	High	Low
B	100 ms	10 ms	12 dB	High	Low	High	High
C	300 ms	30 ms	12 dB	High	High	Low	Low
D	1 s	100 ms	12 dB	High	High	Low	High
E	3 s	300 ms	12 dB	High	High	High	Low
F	10 s	1 s	12 dB	High	High	High	High

Table 5: Time Constants

Full-Scale Sensitivity at DIP switch S1 = OFF				Low Drift High Dyn.	Sensitiv. MSB	Sensitiv.	Sensitiv.
HEX	Voltage Input	Low Drift	High Dyn.	Pin 10	Pin 13	Pin 12	Pin 11
0	100 mV	X	-	Low	Low	Low	Low
1	30 mV	X	-	Low	Low	Low	High
2	10 mV	X	-	Low	Low	High	Low
3	3 mV	X	-	Low	Low	High	High
4	1 mV	X	-	Low	High	Low	Low
5	300 $\mu$ V	X	-	Low	High	Low	High
6	100 $\mu$ V	X	-	Low	High	High	Low
7	30 $\mu$ V	X	-	Low	High	High	High
8	10 mV	-	X	High	Low	Low	Low
9	3 mV	-	X	High	Low	Low	High
A	1 mV	-	X	High	Low	High	Low
B	300 $\mu$ V	-	X	High	Low	High	High
C	100 $\mu$ V	-	X	High	High	Low	Low
D	30 $\mu$ V	-	X	High	High	Low	High
E	10 $\mu$ V	-	X	High	High	High	Low
F	3 $\mu$ V	-	X	High	High	High	High

Full-Scale Sensitivity at DIP switch S1 = ON				Ultra-Stab. Low Drift.	Sensitiv. MSB	Sensitiv.	Sensitiv.
HEX	Voltage Input	Ultra- Stable	Low Drift	Pin 10	Pin 13	Pin 12	Pin 11
0	1 V	X	-	Low	Low	Low	Low
1	300 mV	X	-	Low	Low	Low	High
2	100 mV	X	-	Low	Low	High	Low
3	30 mV	X	-	Low	Low	High	High
4	10 mV	X	-	Low	High	Low	Low
5	3 mV	X	-	Low	High	Low	High
6	1 mV	X	-	Low	High	High	Low
7	300 $\mu$ V	X	-	Low	High	High	High
8	100 mV	-	X	High	Low	Low	Low
9	30 mV	-	X	High	Low	Low	High
A	10 mV	-	X	High	Low	High	Low
B	3 mV	-	X	High	Low	High	High
C	1 mV	-	X	High	High	Low	Low
D	300 $\mu$ V	-	X	High	High	Low	High
E	100 $\mu$ V	-	X	High	High	High	Low
F	30 $\mu$ V	-	X	High	High	High	High

Table 6: Sensitivity

Phase Coarse		Phase (Ph 7)	Phase (Ph 6)	Phase (Ph 5)	Phase (Ph 4)	
HEX	Degree		SUB- D 25 Socket			
	8 Bit	7 Bit	Pin 25	Pin 24	Pin 23	Pin 22
0	0.0	0	Low	Low	Low	Low
1	22.5	45	Low	Low	Low	High
2	45.0	90	Low	Low	High	Low
3	67.5	135	Low	Low	High	High
4	90.0	180	Low	High	Low	Low
5	112.5	225	Low	High	Low	High
6	135.0	270	Low	High	High	Low
7	157.5	315	Low	High	High	High
8	180.0	360	High	Low	Low	Low
9	202.5	405	High	Low	Low	High
A	225.0	450	High	Low	High	Low
B	247.5	495	High	Low	High	High
C	270.0	540	High	High	Low	Low
D	292.5	585	High	High	Low	High
E	315.0	630	High	High	High	Low
F	337.5	675	High	High	High	High

Phase Fine		Phase (Ph 3)	Phase (Ph 2)	Phase (Ph 1)	Phase (Ph 0)	
HEX	Degree		SUB- D 25 Socket			
	8 Bit	7 Bit	Pin 21	Pin 20	Pin 19	Pin 18
0	0.00	0.00	Low	Low	Low	Low
1	1.41	2.81	Low	Low	Low	High
2	2.81	5.62	Low	Low	High	Low
3	4.22	8.44	Low	Low	High	High
4	5.63	11.25	Low	High	Low	Low
5	7.03	14.10	Low	High	Low	High
6	8.44	16.90	Low	High	High	Low
7	9.84	19.70	Low	High	High	High
8	11.25	22.50	High	Low	Low	Low
9	12.70	25.40	High	Low	Low	High
A	14.10	28.20	High	Low	High	Low
B	15.50	31.00	High	Low	High	High
C	16.90	33.80	High	High	Low	Low
D	18.30	36.60	High	High	Low	High
E	19.70	39.40	High	High	High	Low
F	21.10	42.20	High	High	High	High

Table 7: Phase Shifter: 8 bit and 7 bit Resolution

## 9 Mixed Operation

There are two ways of remote control operation depending on the digital signal at the input “Disable Local Switch Control” (Pin 8 of SUB-D 25 socket). High-level applied to this input enables exclusive remote control operation of the settings for time-constant, sensitivity and phase. All manual hexadecimal switches are out of function in this mode. Only the DIP switch settings are relevant as these cannot be remotely controlled.

A mixed mode of operation with digitally remote and manually controlled functions is enabled when Pin 8 is left open or set to “Low”. The internal and external control-bits are then connected by a logical OR function. To ensure a perfect remote control operation in this mixed mode make sure to switch the corresponding hexadecimal-switches to position “0”. The other remaining switches allow for manual operation.

## 10 Advanced Configuration of the Lock-In Amplifier

**Attention:** The following advanced configuration requires opening the housing of the lock-in amplifier. Read the documentation carefully before opening the device. Close the device before putting it back into operation. When changing the configuration pay close attention to the instructions provided further down. A failure in the configuration can damage the device and may expose you to shocks and other hazards.

### 10.1 Opening and Closing the Device

Before opening the device remove the power supply cable and all signal lines. Remove the 2 upper screws from the rear panel and the 2 upper screws from the front panel. You may also slightly loosen the 2 lower screws on the front panel allowing the top lid to open up smoothly.

**Attention:** On older models a grounding wire attached to the main board is fixed by the upper left screw on the rear panel. When loosening the screw a toothed lock washer may fall down on the board of the lock-in amplifier. Remove the toothed lock washer to avoid damage (or short circuit) to the board. On newer models the ground wire is attached by a flat connection directly to the top lid. You can leave this connector plugged while changing the configuration of the lock-in amplifier.

After changing the configuration close the housing by starting with the left upper screw of the rear panel. Insert the toothed lock washer between the case and the rear panel together with the feeder clamp of the grounding wire before mounting the screw. On newer models with a direct grounding connection to the top lid you can mount the left upper screw right away without the need of attaching a washer or feeder clamp first. After fastening the left upper screw mount the right upper screw of the rear panel and the remaining 4 screws of the front panel.

Please bear in mind that the housing is made of relatively soft aluminum. Therefore pay attention when tightening the screws as too much torque may damage the tapped holes.

## 10.2 Optional Sine-Oscillator-Module SOM-1

The optional Sine-Oscillator-Module SOM-1 is especially designed for those applications where a fixed reference frequency is required and an external reference generator is not available to modulate the signal source and drive the reference frequency input of the lock-in amplifier.

The SOM-1 can be set to generate a reference frequency between 5 Hz and 130 kHz without an additional signal generator. The reference frequency and amplitude of the module are adjustable by a trimpot and a jumper setting (see figure 5). The SOM-1 is optimized for fixed frequency operation. Therefore in applications where the reference frequency has to be varied during the measurement within the specified range of the LIA-MV(D)-200 an external reference oscillator should be used.

The SOM-1 requires a supply voltage of  $\pm 15$  V which is supplied by the lock-in amplifier. It is delivered in standard configuration with the following pre-settings:

Frequency: 1.0 kHz

Amplitude:  $1 V_{\text{rms}}$ .

To modify these settings you have to open the device (see chapter 9.1).

First, the user has to decide which reference frequency is adequate for his application. The reference frequency has to be within the specified range of the LIA-MV(D)-200 module. There are 4 ranges for the reference frequency which can be selected by the jumper JP6 on the SOM-1 module (see datasheet of the SOM-1 module for details). The trimpot “frequency adjust” adjusts the frequency within these ranges. The trimpot “amplitude adjust” allows to adjust the amplitude, which can be set from 0 to  $2 V_{\text{rms}}$ . The maximum output current of the oscillator is  $\pm 5$  mA.

Routing the SOM-1 frequency to the BNC socket (labeled “Reference Input”) requires the setting of the relevant jumpers in the jumper field 3 on the adapter-board of the lock-in amplifier (see table 10 and figure 6). Once the jumpers are set correctly the frequency and amplitude can be checked at the BNC socket labeled “REFERENCE INPUT”.

The SOM-1 needs a relatively long warm-up time of up to 30 minutes after switching on the power supply. During this warm-up time the frequency can drift up to 15 %. If a more stable frequency is needed an external reference frequency should be used for synchronization (see table 10).

When the operation mode with synchronization to an externally supplied reference frequency is used, the free running frequency of the SOM-1 module must be adjusted approximately to the reference frequency before connecting the reference signal to the REF.INPUT socket. This ensures that the PLL on the SOM-1 module locks to the fundamental of the reference signal rather than a harmonic.

For further information please see also the datasheet of the SOM-1 module!

### 10.3 Modification of the Input Signal Filters

The LIA-MV(D)-200 series provides adjustable input signal filters. Optimizing the filter settings can increase the dynamic reserve which might be important especially for measurements in noisy environments. The lower and upper cut-off frequency can be set independently by a low pass and a high pass filter according to the following table (see figure 5 for the jumper positions):

lower cut-off frequency (-3dB)		JP3	upper cut-off frequency (-3dB)	JP1	JP2
Model -L	Model -H				
0.2 Hz*	2 Hz*	3 – 4	100 Hz	1 – 2	1 – 2
1.0 Hz	10 Hz	1 – 3	1 kHz	3 – 4	3 – 4
10.0 Hz	100 Hz	2 – 4	10 kHz	5 – 6	5 – 6
100.0 Hz	1 kHz	3 – 5	100 kHz	7 – 8	7 – 8
1.0 kHz	10 kHz	4 – 6	> 1 MHz*	free	free

\* standard configuration

Table 8: Setting of the Signal Filters: Jumpers JP1-JP3

### 10.4 Setting the Working Frequency Range (H-Models Only)

The factory setting for the H-model lock-in amplifiers provides a working frequency range from 50 Hz to 120 kHz with a phase shifter resolution of 7 bit. The switch „S2“ for selecting the 2f-mode is inoperative. If you need 2f-mode or a phase shifter resolution of 8 bit you have to change the jumpers in field 4 (see table 9). Please note that this will limit the working frequency to a range of 50 Hz to ca. 60 kHz.

Model	Frequencies at Reference input	Lock-In Mode	Jumper Block JP4	Position DIP switch S2	Phase Shifter Resolution
-L	$5 \text{ Hz} \leq f \leq 10\text{kHz}$	1f	1 – 2	1f	8 bit
-L	$5 \text{ Hz} \leq f \leq 10\text{kHz}$	2f	1 – 2	2f	7 bit
-H	$50 \text{ Hz} \leq f \leq 120\text{kHz}$ (factory setting)	1f	3 – 4 and 5 – 6	irrelevant	7 bit
-H	$50 \text{ Hz} \leq f \leq 60\text{kHz}$	1f	1 – 2	1f	8 bit
-H	$50 \text{ Hz} \leq f \leq 60\text{kHz}$	2f	1 – 2	2f	7 bit

Table 9: Jumper Settings for Different Working Frequency Ranges and Operating Modes



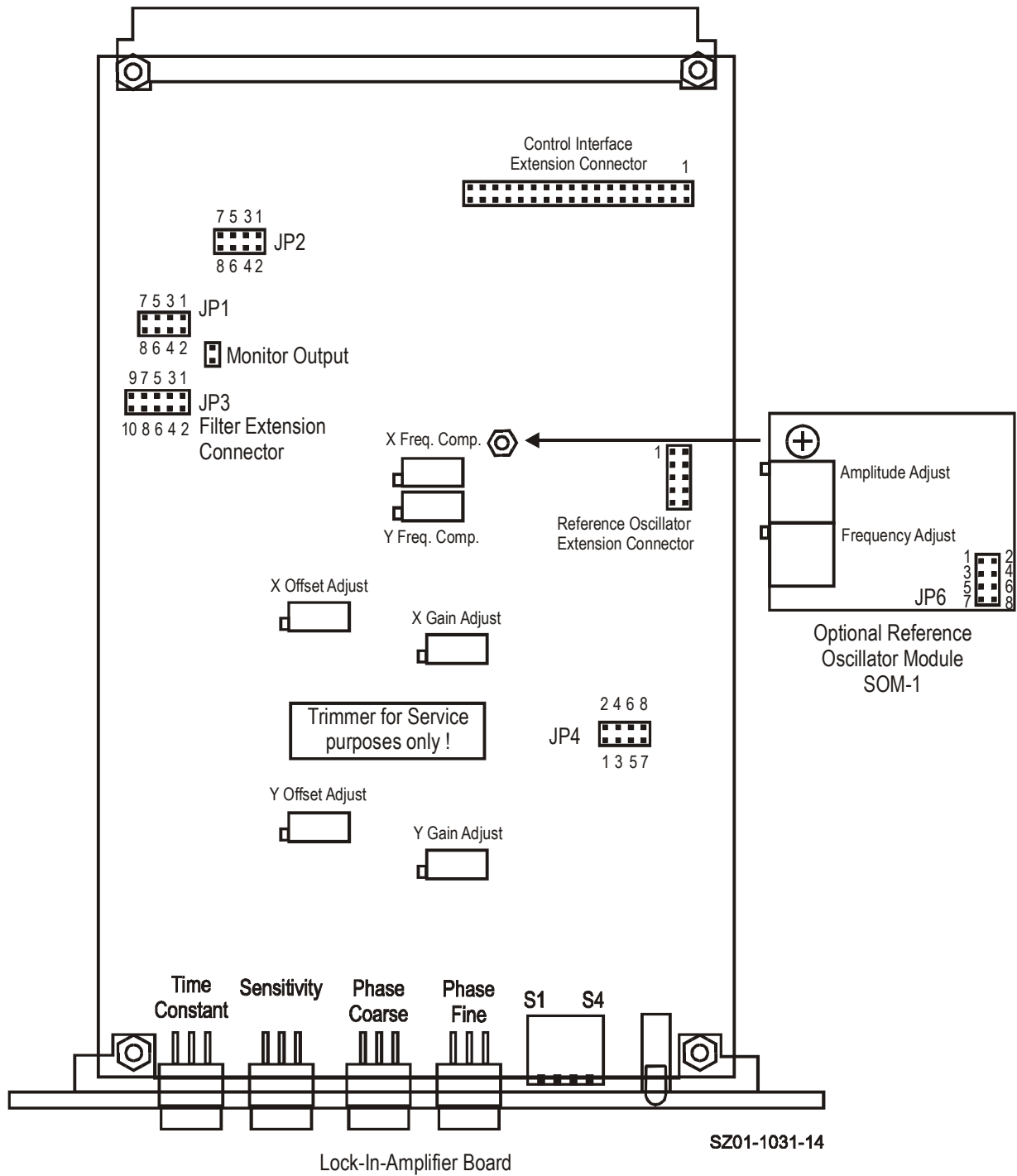


Figure 5: Overview of the Jumper Positions

### 10.5 Changing the Assignment of the BNC Sockets

The assignment of the BNC sockets on the rear panel can be changed and adapted to the particular operation conditions.

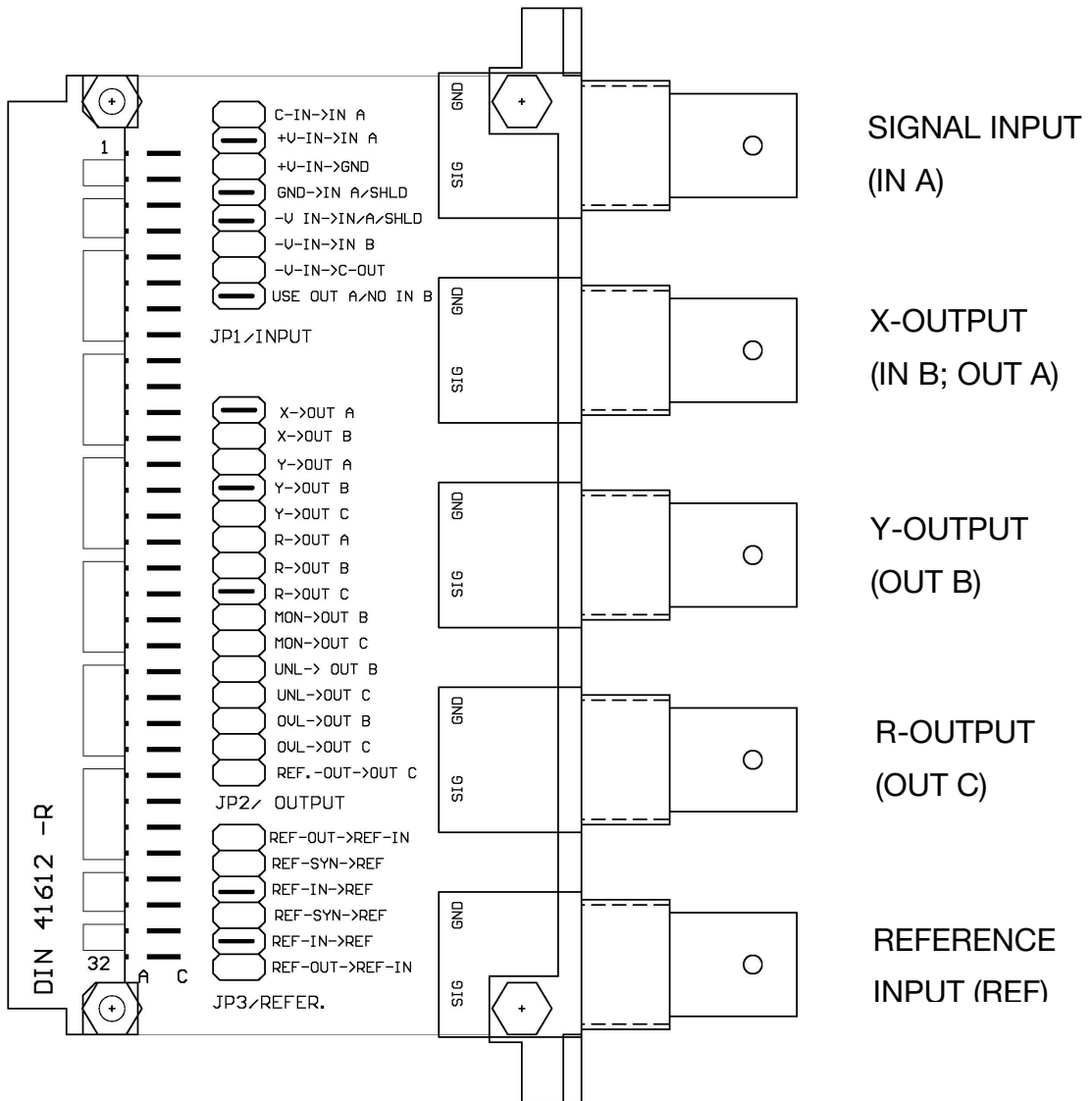


Figure 6: View of the Jumper Field of the Adapter Board for a Dual Phase Model LIA-MVD-200 Showing Standard Configuration without SOM-1 Sine Oscillator Module.

Remark: Single phase models LIA-MV-200 do not contain the BNC sockets “Y-OUTPUT” and “R-OUTPUT”.

The following options for special configurations correspond mostly to dual phase models LIA-MVD-200.

### 10.5.1 Options for the Assignment of the BNC Socket “REFERENCE INPUT”

Socket Function	Set Jumper	Jumper Field
An external reference frequency is used. (standard configuration without SOM-1 module)	REF-IN ->REF 2x	JP3
The signal of the SOM-1 module is used as internal reference frequency and is externally available too. (standard configuration with SOM-1 module)	REF-OUT ->REF-IN 2x REF-IN ->REF 2x	JP3 JP3
The signal of the SOM-1 module is used as internal reference frequency and can be synchronized with an external signal generator.  The reference signal of the SOM-1 module is also externally available at the socket “R-OUTPUT”. (dual phase models only)	REF-SYN -> REF 2x REF-OUT -> OUT C 1x REF-OUT -> REF-IN 2x	JP3 JP2 JP3

Table 10: Assignments of the BNC Socket “REFERENCE INPUT”

**10.5.2 Options for the Assignment of the BNC Socket “SIGNAL INPUT”**

Socket Function	Set Jumper		Jumper Field
AC coupled voltage input, single ended The socket “X OUTPUT” is used as output “OUT A” (standard configuration)	+V-IN -> IN A	1x	JP1
	GND -> IN A/SHLD	1x	JP 1
	-V-IN -> IN A/SHLD	1x	JP 1
	USE OUT A/NO IN B	1x	JP 1
AC coupled voltage input, differential, 1x BNC The center conductor and the outer conductor of the socket “SIGNAL INPUT” are used as differential input. The outer conductor is NOT internally connected to ground The socket “X OUTPUT” is used as output “OUT A”	+V-IN -> IN A	1x	JP 1
	-V-IN -> IN A/SHLD	1x	JP 1
	USE OUT A/NO IN B	1x	JP 1
AC coupled voltage input, differential, 2x BNC The center conductors of the sockets “SIGNAL INPUT” and “X-OUTPUT” are used as symmetric signal input. The outer conductors of the two sockets are grounded. The BNC socket “Y-OUTPUT” is used as X-Output for dual phase models. * For single phase models PIN 5 of the SUB-D 25 socket must be used as output.	+V-IN -> IN A	1x	JP 1
	GND -> IN A/SHLD	1x	JP 1
	-V-IN -> IN B	1x	JP 1
	X -> OUT B	1x	JP 2
Current input, asymmetric (single ended) The socket “SIGNAL INPUT” is set as current input with a transimpedance gain of -100 kV/A (inverting) The socket “X OUTPUT” is used as output “OUT A”	C-IN -> IN A	1x	JP 1
	GND -> IN A/SHLD	1x	JP 1
	-V-IN -> C-OUT	1x	JP 1
	+V-IN -> GND	1x	JP 1
	USE OUT A/NO IN B	1x	JP 1

Table 11: Assignment of the BNC Socket “SIGNAL INPUT”

Note: When using current input with low input ranges, the monitor output may be disabled by opening the soldering jumper at the board (near JP1, see image 4) to prevent from recoupling.

\* When setting jumpers, only one output signal can be connected to one BNC socket (see remark under table 12).

### 10.5.3 Options for the Assignment of the „OUTPUT” BNC Sockets

Socket Function	Set Jumper	Jumper Field
The X-output signal is connected to “X-OUTPUT” (standard configuration)	X -> OUT A      1x	JP2
	USE OUT A/NO IN B      1x	JP1
The X-output signal is connected to “Y-OUTPUT”	X -> OUT B      1x	JP2
The Y-output signal is connected to “Y-OUTPUT” (standard configuration)	Y -> OUT B      1x	JP2
The Y-output signal is connected to “X-OUTPUT”	Y -> OUT A      1x	JP2
	USE OUT A/NO IN B      1x	JP1
The Y-output signal is connected to “R-OUTPUT”	Y -> OUT C      1x	JP2
The R-output signal is connected to “R-OUTPUT” (standard configuration)	R -> OUT C      1x	JP2
The R-output signal is connected to “X-OUTPUT”	R -> OUT A      1x	JP2
	USE OUT A/NO IN B      1x	JP1
The R-output signal is connected to “Y-OUTPUT”	R -> OUT B      1x	JP2
The monitor signal is connected to “Y-OUTPUT”***	MON -> OUT B      1x	JP2
The monitor signal is connected to “R-OUTPUT”***	MON -> OUT C      1x	JP2
The unlocked signal is connected to “Y-OUTPUT”	UNL -> OUT B      1x	JP2
The unlocked signal is connected to “R-OUTPUT”	UNL -> OUT C      1x	JP2
The overload signal is connected to “Y-OUTPUT”	OVL -> OUT B      1x	JP2
The overload signal is connected to “R-OUTPUT”	OVL -> OUT C      1x	JP2

Table 12: Options for the assignment of the BNC output sockets X, Y and R

Remark: When setting jumpers, only one output signal can be connected to one BNC socket. If e.g. the jumper “X -> OUT B” (output signal X connected to BNC socket B) is installed, no other output signal (Y, R, MON, UNL, OVL) is allowed to be connected to the BNC socket “OUT B”.

\*\* In order to route the monitor signal to one of the BNC sockets, the solder jumper “Monitor Output” on the LIA board (near JP1, see figure 5) must be closed. Please pay attention to the note below table 11.

## 11 Dimensions

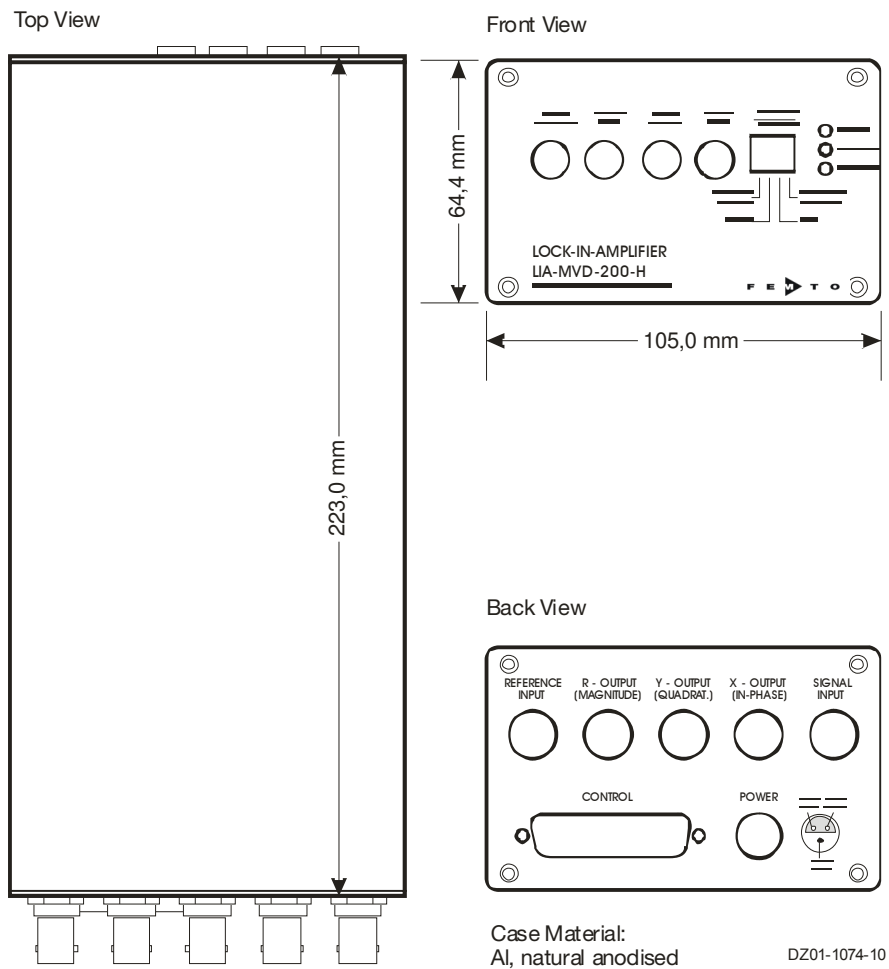


Figure 7: Dimensions

## 12 Block Diagram

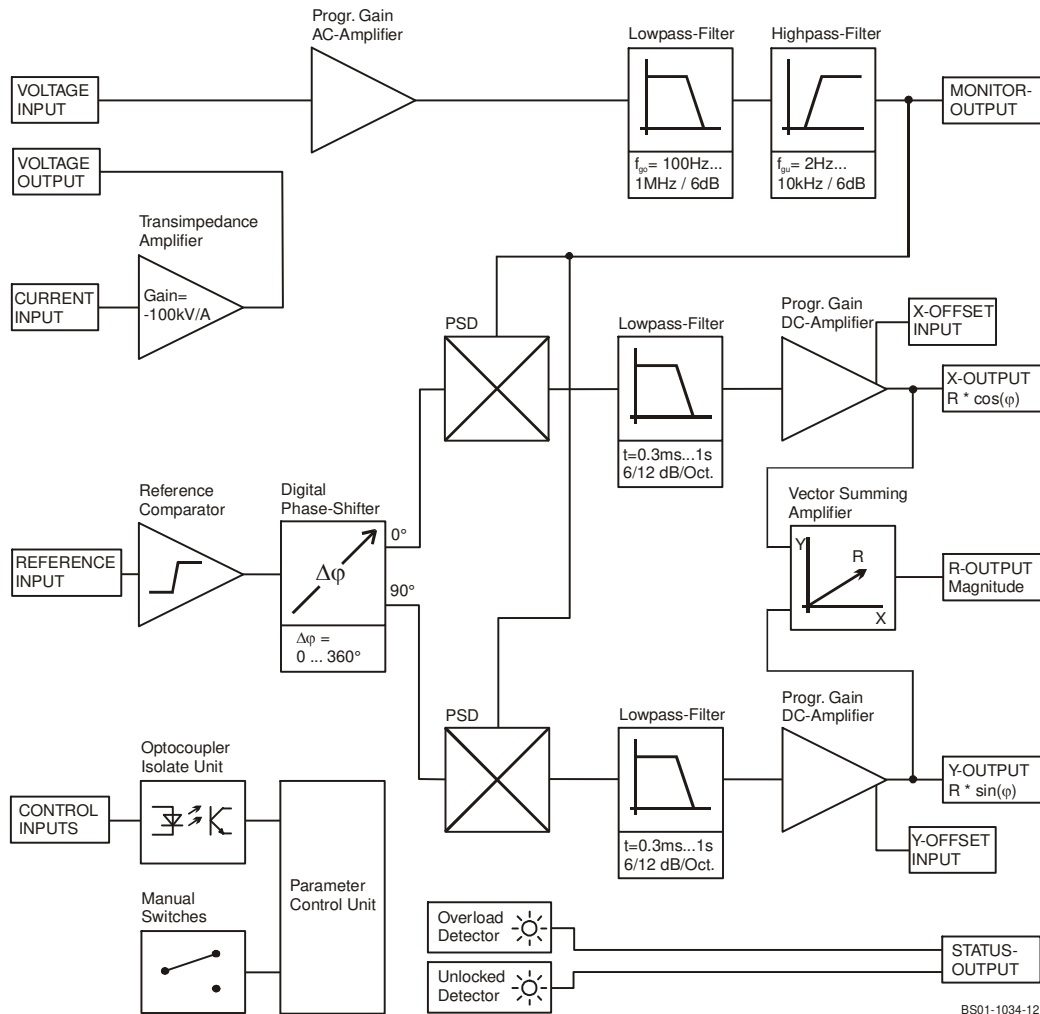


Figure 8: Block Diagram of the LIA-MVD-200-H